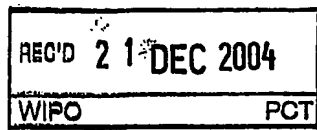


(2 1. 12. 04)



INVESTOR IN PEOPLE

The Patent Office
Concept House
Cardiff Road
Newport
South Wales
NP10 8QQ

PRIORITY DOCUMENT

SUBMITTED OR TRANSMITTED IN
COMPLIANCE WITH RULE 17.1(a) OR (b)

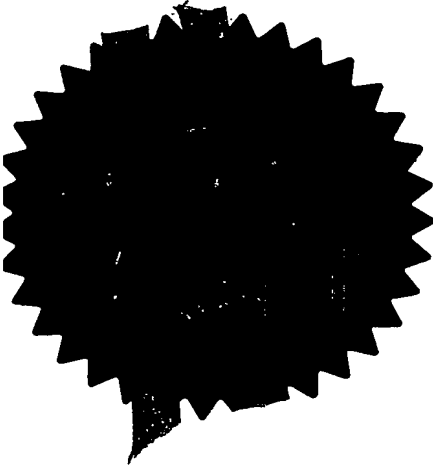
PCT/IB04/3939

I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation & Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named in this certificate and any accompanying documents has re-registered under the Companies Act 1980 with the same name as that with which it was registered immediately before re-registration save for the substitution as, or inclusion as, the last part of the name of the words "public limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

In accordance with the rules, the words "public limited company" may be replaced by p.l.c., plc, P.L.C. or PLC.

Re-registration under the Companies Act does not constitute a new legal entity but merely subjects the company to certain additional company law rules.



Signed

Atkins

Dated 11 October 2004

The
Patent
Office

THE PATENT OFFICE
H

1/77
15-0063/2553172-1/002319
*0177700 0.00-0326862.0

Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

18 NOV 2003

LONDON

The Patent Office

Cardiff Road
Newport
Gwent NP9 1RH

1. Your reference

SC12938EI/CJH/GBRI/EJL/ROZEN

2. Patent application number

(The Patent Office will fill in this part)

0326862.0

3. Full name, address and postcode of the or of each applicant (underline all surnames)

MOTOROLA, INC
1303 EAST ALGONQUIN ROAD,
SCHAUMBURG, ILLINOIS 60196,
U.S.A.

Patents ADP number (if you know it)

00201107004

00615336007

If the applicant is a corporate body, give the country/state of its incorporation

U.S.A.

DELAWARE

4. Title of the invention

METHOD AND DEVICE FOR REGULATING A VOLTAGE SUPPLY TO A SEMICONDUCTOR DEVICE

5. Name of your agent (if you have one)

"Address for service" in the United Kingdom to which all correspondence should be sent (including the postcode)

HARRISON, CHRISTOPHER
EUROPEAN INTELLECTUAL PROPERTY DEPARTMENT
MIDPOINT
ALENCON LINK
BASINGSTOKE
HAMPSHIRE RG21 7PL
UK
ADP NO. 00001180006 ✓

Patents ADP number (if you know it)

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and (if you know it) the or each application number

Country

Priority application number
(if you know it)

Date of filing
(day / month / year)

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application

Date of filing
(day / month / year)

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? (Answer 'Yes' if:

☒ YES ☐ NO

- a) any applicant named in part 3 is not an inventor, or
 - b) there is an inventor who is not named as an applicant, or
 - c) any named applicant is a corporate body.
- See note (d))

Patents Form 1/77

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form

Description 9 —

Claim(s) 3 —

Abstract 1 —

Drawing(s) 2 + 2 Jim —

10. If you are also filing any of the following, state how many against each item.

Priority documents

Translations of priority documents

Statement of inventorship and right to grant of a patent (Patents Form 7/77) 4 —

Request for preliminary examination and search (Patents Form 9/77) 1 —

Request for substantive examination (Patents Form 10/77) 1 —

Any other documents 1 x FEE SHEET —
(please specify)

11. I/We request the grant of a patent on the basis of this application.

Signature

Date

18/11/2003

12. Name and daytime telephone number of person to contact in the United Kingdom

HARRISON, CHRISTOPHER

Eliza LAURIE

01256 790763

Warning

After an application for a patent has been filed, the Comptroller of the Patent Office will consider whether publication or communication of the invention should be prohibited or restricted under Section 22 of the Patents Act 1977. You will be informed if it is necessary to prohibit or restrict your invention in this way. Furthermore, if you live in the United Kingdom, Section 23 of the Patents Act 1977 stops you from applying for a patent abroad without first getting written permission from the Patent Office unless an application has been filed at least 6 weeks beforehand in the United Kingdom for a patent for the same invention and either no direction prohibiting publication or communication has been given, or any such direction has been revoked.

Notes

- If you need help to fill in this form or you have any questions, please contact the Patent Office on 0645 500505.
- Write your answers in capital letters using black ink or you may type them.
- If there is not enough space for all the relevant details on any part of this form, please continue on a separate sheet of paper and write "see continuation sheet" in the relevant part(s). Any continuation sheet should be attached to this form.
- If you have answered "Yes" Patents Form 7/77 will need to be filed.
- Once you have filled in the form you must remember to sign and date it.
- For details of the fee and ways to pay please contact the Patent Office.

DUPLICATE

5

METHOD AND DEVICE FOR REGULATING A VOLTAGE SUPPLY TO A SEMICONDUCTOR DEVICE

The present invention relates to a method and device for regulating a voltage supply to a semiconductor device.

10

As the demand for portable electronic devices has increased so correspondingly has the requirement for increased battery life and processor performance.

15

While processor performance has continued to increase at a rapid rate, improvements in battery performance have not.

20

Additionally, in many cases the increase in processor performance has resulted in an increased power usage, which could result in many cases in a reduced battery life.

Consequently, there is a continuing drive to reduce power usage.

25

One solution that manufactures have used to reduce power usage within portable electronic devices has included temporarily turning off unneeded peripherals; blocks of on-chip memory and, during idle periods, the processor itself.

30

Another solution involves lowering the supply voltage to an integrated circuit to the lowest voltage that is necessary to maintain the performance of the integrated circuit. This solution is based on the principle that the specified voltage supply requirements for an integrated circuit are based upon worst case conditions, for example worst case operational temperature and the quality of the

5 production process(i.e. manufactured process corner), whereas actual conditions are normally better than these.

10 One technique for determining the lowest voltage that would be needed to maintain the performance of an integrated circuit is to decrease the integrated circuit supply voltage in steps until the integrated circuit is measured to be operating just within a predetermined performance. However, the time taken to perform this operation can still result in a large waste of power.

It is desirable to improve this situation.

15

In accordance with a first aspect of the present invention there is provided a device for regulating a voltage supply to a semiconductor device according to claim 1.

20

This provides the advantage of allowing a minimum voltage supply to be determined quickly and without having to perform performance limit calculations.

25 In accordance with a second aspect of the present invention there is provided a method for regulating a voltage supply to a semiconductor device according to claim 8.

An embodiment of the invention will now be described, by way of example, with reference to the drawings, of which:

30

Figure 1 illustrates an arrangement for regulating a voltage supply to a semiconductor device according to an embodiment of the present invention;

5 Figure 2 illustrates a look-up table according to an embodiment of the present invention

Figure 3 illustrates a graphical representation of a look-up table according to an embodiment of the present invention.

10

Figure 1 shows an integrated circuit 100, a power management module 101 having a voltage supply regulator 112 for providing a supply voltage to the integrated circuit 100, a software module 102 for controlling the regulation of the supply voltage to the integrated circuit 100 and a memory module 103 having a
15 look-up table 104 for storing performance data associated the integrated circuit 100.

The integrated circuit includes a reference counting circuit 106, a ring oscillator 107 that acts as a reference circuit, three comparators 108, 109, 110 and
20 a look-up table register 111. It should be noted, however, that the comparators 108, 109, 110 and the look-up table register 111 could be located of chip from the integrated circuit 100.

The ring oscillator 107 (i.e. reference circuit) is arranged to generate a free
25 running reference clock signal that is provided to the reference counting circuit 106. The reference circuit 107 is a subset of the circuits formed on the integrated circuit 100 and is used as a measure of the performance of the integrated circuit 100. The purpose of using the reference circuit 107 is to determine the performance of the integrated circuit 100 is to minimise the complexity of the
30 device for regulating the voltage supply to the integrated circuit 100. However, it could also be possible to measure the operating performance of all of the circuits on the integrated circuit 100.

5 The frequency of the reference circuit 107 clock signal is related to how the reference circuit 107 is performing, and is dependent upon the operating conditions of the reference circuit 107, such as the operating temperature of the integrated circuit, the supply voltage supplied to the integrated circuit 100 and the manufactured process corner.

10 As stated above the reference circuit clock signal is a clock signal that is based upon the process corner case, the environmental conditions and the voltage of the integrated circuit 100. This is in contrast to the operating frequency of the integrated circuit 100, which is the clock rate to which the integrated circuit is
15 working too.

 The reference counting circuit 106 measures the clock signal, which as stated above is a reflection of the performance of the reference circuit 107, and provides the measurements to the comparators 108, 109, 110.

20 The comparators 108, 109, 110 are coupled to the look-up table register 111, with the look-up table register 111 also being coupled to the memory module 103 for accessing information stored in the look-up table 104 contained within the memory module 103.

25 As shown in figure 2 the look-up table 104, within the memory module 103, is preloaded with a set of reference circuit count values, where each set of reference circuit count values is associated with a respective supply voltage. Each set of reference circuit count values define a range of performance for the reference
30 circuit 107, where, in this embodiment, the reference circuit count values differ for the different supply voltages, a graphical representation of the data is shown in figure 3.

5 Each set of reference circuit count values stored within the look-up table 104 defined three performance markers (i.e. three levels of performance of the integrated circuit). The first level 201, the upper performance limit, indicates the reference circuit count value that corresponds to the upper performance limit for the integrated circuit 100 at a specified voltage. The second level 202, the lower
10 performance limit, indicates the reference circuit count value that corresponds to the lowest acceptable performance level for the integrated circuit 100 at a specified voltage. The third level 203, the critical lower performance level, indicates a reference circuit count value that corresponds to a level of performance at which logic operation failures within the integrated circuit 100 could occur for a
15 specified voltage.

The values for the three performance levels 201, 202, 203 include a performance guard margin, which corresponds to an additional safety margin added to each of the determined performance levels for the reference circuit 105
20 to account for possible differences between the performance of the reference circuit 107 and the integrated circuit 100 as a whole. If the performance of the integrated circuit 100 as a whole was being measured, rather than just the reference circuit 107, it would be unnecessary to include a guard margin/safety margin within the performance level values.

25

By way of illustration, figure 2 shows that for the current embodiment nine supply voltages 204 for the integrated circuit 100 have been defined where each supply voltage is associated with a respective performance range (i.e. a range of reference circuit count values), where the performance range for the first voltage of
30 1.2 provides a reference circuit count value for the upper performance limit of 290 counts, a reference circuit count value for the lower performance limit of 275 counts and a reference circuit count value for the critical lower performance level of 264 counts.

5 The performance limits stored in the look-up table 104 are based on two main parameters: IR (i.e. current resistance) drop value (voltage reduction due to current flow through metal interconnects) and the accuracy of the voltage supply regulator 112.

10 The critical lower performance level 203 is set by the minimal required voltage level and IR drop value, where IR drop value depends on existing absolute supply voltage level. The critical lower performance level 203 is set such that if the maximum IR drop occurs the supply voltage inside the integrated circuit 100 would be so low that the most constrained delay paths might begin to malfunction.

15 The lower performance limit 202 is higher than the critical lower performance level 203 by a value proportional to the voltage raise of one minimum step of the voltage supply regulator 112 plus some spare margin.

20 The higher performance limit 201 is higher than the lower performance limit 202 by a value proportional to a voltage raise of one and the half voltage steps of the voltage supply regulator 112 plus some spare margin.

25 The software module 102, which receives information from the power management module 101 as to the voltage supply being provided to the integrated circuit 100, is arranged to load the three reference circuit count performance values associated with the supplied voltage into the look-up table register 111.

30 The look-up table register 111 is arranged to provide the upper performance level value and the lower performance level reference circuit count value to the first comparator 108 and second comparator 109 respectively and the critical lower performance level reference circuit count value to the third comparator 110.

5 The first comparator 108 compares the measured reference count value received from the reference counting circuit 106 with the reference circuit count value received from the look-up table register 111 (i.e. the upper performance level reference circuit count value).

10 If the measured reference count value falls below the upper performance level reference circuit count value the first comparator 108 provides no output.

15 If the measured reference count value is above the upper performance level reference circuit count value (i.e. the supply voltage is unnecessarily high) the first comparator 108 issues an interrupt request to the software module 102 requesting a voltage decrease. On receipt of the interrupt request the software module 102 initiates an instruction to the power management module 101 to lower the voltage supply to the integrated circuit 100 to the next lower voltage supply level within the look-up table and the software module 102 initiates the loading of the three
20 reference circuit count performance values associated with the new supplied voltage into the look-up table register 111.

25 The second comparator 109 compares the measured reference circuit count value received from the reference counting circuit 106 with the reference circuit count value received from the look-up table register 111 (i.e. the lower performance level reference circuit count value).

30 If the measured reference count value is higher than the lower performance level reference circuit count value the second comparator 109 provides no output.

 If the measured reference count value is below the lower performance level reference circuit count value (i.e. the supply voltage is too low) the second comparator 109 issues an interrupt request to the software module 102 requesting a voltage increase. On receipt of the interrupt request the software module 102

5 initiates an instruction to the power management module 101 to increase the voltage supply to the integrated circuit 100 to the next highest voltage supply level within the look-up table and the software module 102 initiates the loading of the three reference circuit count performance values associated with the new supplied voltage into the look-up table register 111.

10

The third comparator 110 compares the measured reference circuit count value received from the reference counting circuit 106 with the reference circuit count value received from the look-up table register 111 (i.e. the critical lower performance reference circuit count value).

15

If the measured reference circuit count value falls below the critical lower performance level reference circuit count value, which is placed at a lower count level to the lower performance level, this could indicate that a previous request to increase the voltage supply to the integrated circuit 100 is occurring too slowly and/or the operating environment conditions are degrading at a fast rate. In response to the measured reference circuit count value falling below the critical lower performance level the third comparator 110 issues a high priority interrupt request to the software module 102 requesting a voltage increase. On receipt of the high priority interrupt request the software module places a high priority instruction to the power management module 101 requesting an increase in the voltage supply to the integrated circuit 100 to the next higher voltage supply level and, if not already performed as a result of any previous voltage request interrupts from the second comparator 109, the software module 102 initiates the loading of the three reference circuit count performance values associated with the new supply voltage to the look-up table register 111.

It will be apparent to those skilled in the art that the disclosed subject matter may be modified in numerous ways and may assume many embodiments other than the preferred forms specifically set out as described above, for example the above embodiments could be arranged such that the look-up table 104 could have

- 5 more or less than three performance levels and the change in voltage could be to voltage levels other than the next value up or down from the current voltage value within the look-up table 104, rather than the comparators 108, 109, 110 being arranged to send a signal when a performance level has been reached. the comparators 108, 109, 110 could be arranged to stop sending a signal when a
- 10 performance level has be reached.

5 CLAIMS

- 10 1. A device for regulating a voltage supply to a semiconductor device, the device comprising memory for storing a plurality of performance ranges, wherein the respective performance ranges are associated with a respective supply voltage; means for measuring the performance of the semiconductor device; and a regulator for modifying the supply voltage to the semiconductor device if the measured performance of the semiconductor device is not within a predetermined portion of the performance range associated with the voltage supplied to the semiconductor device.
15
2. A device according to claim 1, wherein the performance range is defined to have an upper performance limit such that if the measured performance of the semiconductor device is above the upper performance limit the regulator is arranged to reduce the voltage supplied to the semiconductor device.
20
- 25 3. A device according to claim 1 or 2, wherein the performance range is defined to have a lower performance limit such that if the measured performance of the semiconductor device is below the lower performance limit the regulator is arranged to increase the voltage supplied to the semiconductor device.
- 30 4. A device according to any of claim 1 to 3, wherein the performance range is defined to have a critical lower performance limit such that if the measured performance of the semiconductor device is below the critical lower

5 performance limit the regulator is arranged to increase the voltage supplied to the semiconductor device.

10 5. A device according to any of claims 1 to 4, wherein the means for measuring the performance is arranged to measure the performance of the semiconductor device by measuring the performance of a reference circuit that forms part of the semiconductor device.

15 6. A device according to claim 5, wherein the plurality of performance ranges are arranged to include a performance guard margin to compensate for differences between the measured performance of the reference circuit and the actual performance of the complete integrated circuit.

20 7. A device according to any preceding claim, further comprising a ring oscillator, wherein the means for measuring the performance measures the frequency of the ring oscillator for providing a measure of the performance of the integrated circuit.

25 8. A method for regulating a voltage supply to a semiconductor device, the method comprising storing a plurality of performance ranges, wherein the respective performance ranges are associated with a respective supply voltage; measuring the performance of the semiconductor device; and modifying the supply voltage to the semiconductor device if the measured performance of the semiconductor device is not within a predetermined portion of the performance range associated with the voltage supplied to the semiconductor device.

30



5 9. A device substantially as herein described with reference to the accompanying figures.

10. A method substantially as herein described with reference to the accompanying figures.

10

5 **ABSTRACT****METHOD AND DEVICE FOR REGULATING A VOLTAGE SUPPLY TO A SEMICONDUCTOR DEVICE**

10 A device for regulating a voltage supply to a semiconductor device, the device comprising memory for storing a plurality of performance ranges, wherein the respective performance ranges are associated with a respective supply voltage; means for measuring the performance of the semiconductor device; and a regulator for modifying the supply voltage to the semiconductor device if the measured performance of the semiconductor device is not within a predetermined
15 portion of the performance range associated with the voltage supplied to the semiconductor device.

20 (Figure 1)

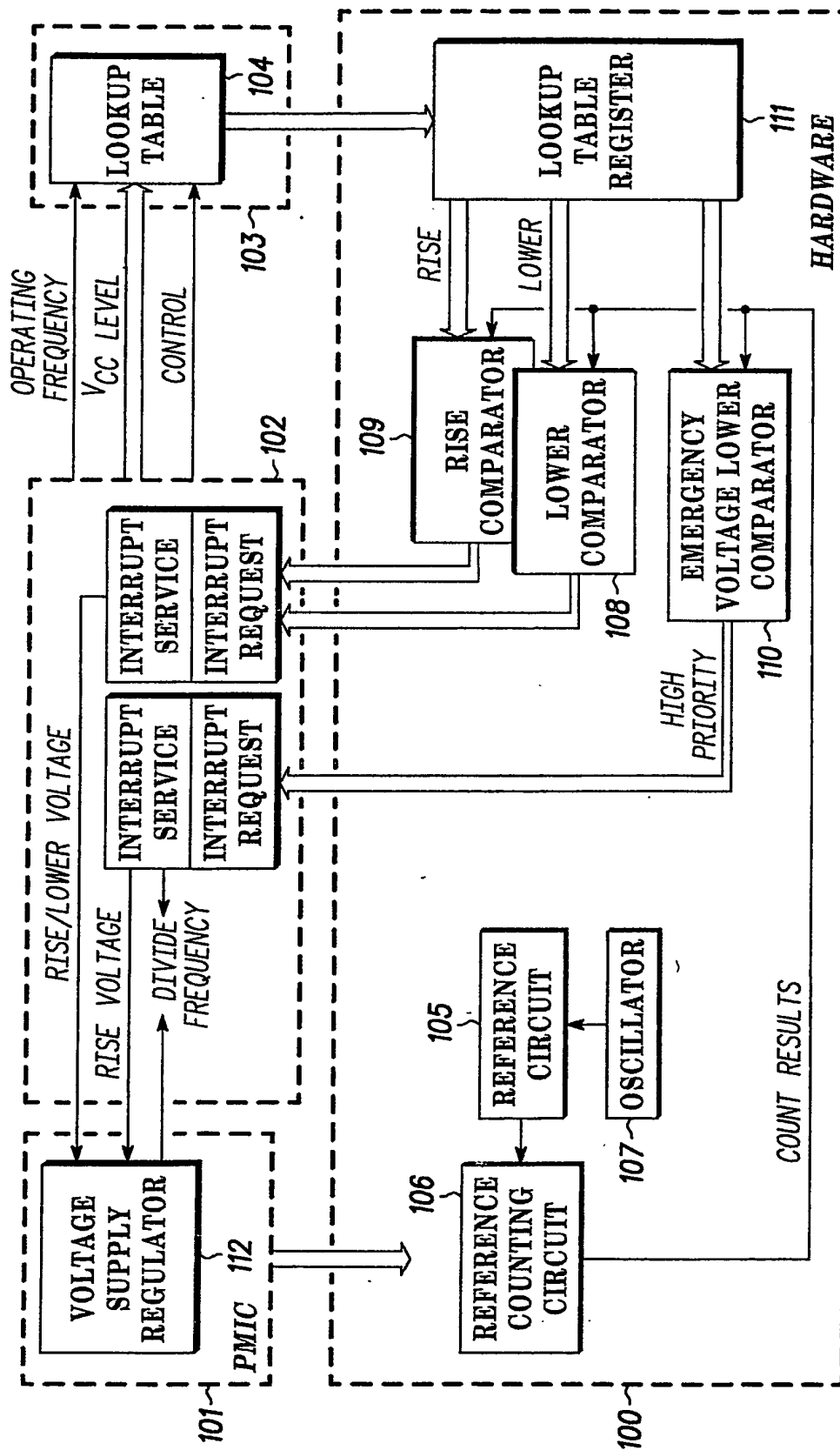
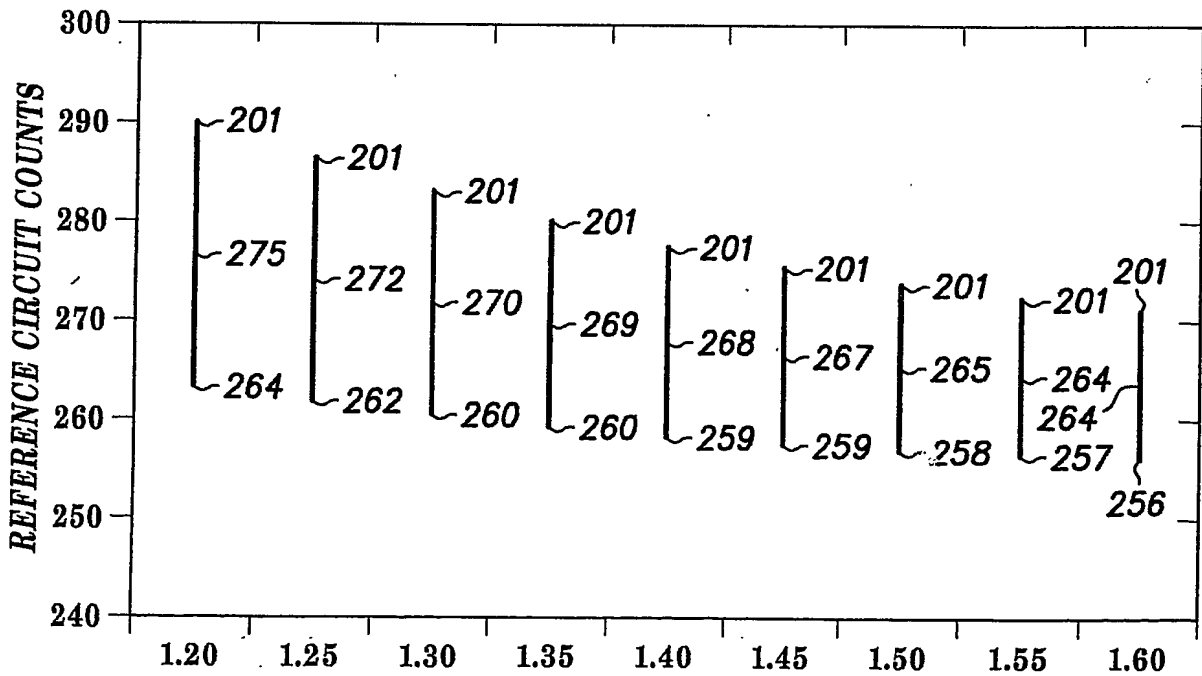


FIG. 1

204 VOLTAGE	203 FREQUENCY DIVISION PLUS RISE VOLTAGE	202 RISE VOLTAGE	201 LOWER VOLTAGE
1.20	263	276	291
1.26	262	273	287
1.30	261	271	283
1.35	260	269	280
1.40	259	267	277
1.45	258	266	275
1.50	258	265	273
1.55	257	264	272
1.60	257	264	271

FIG. 2*FIG. 3*

204

PCT/IB2004/003939



**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKEWED/SLANTED IMAGES**
- ☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☒ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER: _____**

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.